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| 09/616,086 | 07/14/2000 | Masaki Tamaru | 32811 | 6585 |

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| EXAMINER |
|---|
| VU, HUNG K |

| ART UNIT | PAPER NUMBER |
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DATE MAILED: 11/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/616,086 | Applicant(s) TAMARU ET AL. | |
|---|---|---|---|
| | Examiner Hung K. Vu | Art Unit 2811 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *31 July 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-17 and 20-31* is/are pending in the application.

4a) Of the above claim(s) *4,5,7-16 and 20-31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6 and 17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 17 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 17, lines, 2 – 4, the phrase "said first and second conductive layers are filled in the first and second through-holes, and the upper ends thereof are connected to the first and second conductive layers" is unclear as to how the first and second conductive layers are filled in the first and second through-holes can have the upper ends which are connected to the first and second conductive layers.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 – 3, 6 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Takahashi et al. (PN 5,311,048, of record).

Takahashi et al. discloses, as shown in Figures 1 and 7, a semiconductor device comprising,

a first conductive layer (12) formed of a surface of a semiconductor substrate;

a second conductive layer (12) which is formed close to the first conductive layer, wherein

the distance between adjacent conductive structures (the first conductive layer (12) and the second conductive layer (12)) is commonly determined by the permittivity of the insulating layer (10,13) encapsulating the conductive structures. Please note that permittivity of the insulating layer controls the capacitance between adjacent conductive structures. Effective control of this capacitance is essential in achieving the optimum electrical characteristics of a semiconductor device. So this particular limitation is held inherent in that the distance between the adjacent conductive structures is determined by the permittivity of the insulating layer. In alternative, this limitation (the distance between the adjacent conductive structures being determined by the permittivity of the insulating layer) deals with how the claimed device is made. Therefore, the claimed device must be directed to the product per se, no matter how actually made.

With regard to claim 2, Takahashi et al. discloses the second conductive layer is made of a conductive film being filled in a through hole being located close to the first conductive layer and passing through at least a part of the insulating film; and the first and second conductive layers are connected to first and second potentials (Vss, Vcc), respectively, and a capacitor, which extends in the depth direction of the through hole, is formed by using the insulating inter-layer film interposed between the first conductive layer and the second conductive layer within the through hole.

With regard to claim 3, Takahashi et al. discloses the through hole comprises a second through hole being electrically connected to a semiconductor region or a wiring region only at either of the opened ends thereof.

With regard to claim 6, Takahashi et al. discloses the first conductive layer is formed within a first through-hole being separated by a predetermined distance from the through-hole, whereby a vertical capacitor, which extends in the depth direction of the through-hole, is formed by the first and second conductive layers (12,12) and the insulating film (10,13) interposed between the first and second conductive layers.

With regard to claim 17, Takahashi et al. discloses the first and second conductive layers are filled in the first and second through-holes, and the upper ends thereof are connected to the first and second conductive layers, and the spatial intervals in the arrays of the first and second conductive layers are smaller than those in the arrays of the first and second through-holes.

3. Claims 1 – 3, 6 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakanishi et al. (PN 4,954,877, of record).

Nakanishi et al. discloses, as shown in Figure 1B, a semiconductor device comprising,

a first conductive layer (15) formed of a surface of a semiconductor substrate;

a second conductive layer (15') which is formed close to the first conductive layer, wherein

the distance between adjacent conductive structures (the first conductive layer (15) and the second conductive layer (15')) is commonly determined by the permittivity of the insulating layer (3) encapsulating the conductive structures. Please note that permittivity of the insulating layer controls the capacitance between adjacent conductive structures. Effective control of this capacitance is essential in achieving the optimum electrical characteristics of a semiconductor device. So this particular limitation is held inherent in that the distance between the adjacent conductive structures is determined by the permittivity of the insulating layer. In alternative, this limitation (the distance between the adjacent conductive structures being determined by the permittivity of the insulating layer) deals with how the claimed device is made. Therefore, the claimed device must be directed to the product per se, no matter how actually made.

With regard to claim 2, Nakanishi et al. discloses the second conductive layer is made of a conductive film being filled in a through hole being located close to the first conductive layer and passing through at least a part of the insulating film; and the first and second conductive layers are connected to first and second potentials (+,-), respectively, and a capacitor, which extends in the depth direction of the through hole, is formed by using the insulating inter-layer film interposed between the first conductive layer and the second conductive layer within the through hole.

With regard to claim 3, Nakanishi et al. discloses the through hole comprises a second through hole being electrically connected to a semiconductor region or a wiring region only at either of the opened ends thereof.

With regard to claim 6, Nakanishi et al. discloses the first conductive layer is formed within a first through-hole being separated by a predetermined distance from the through-hole, whereby a vertical capacitor, which extends in the depth direction of the through-hole, is formed by the first and second conductive layers (15,15') and the insulating film (3) interposed between the first and second conductive layers.

With regard to claim 17, Nakanishi et al. discloses the first and second conductive layers are filled in the first and second through-holes, and the upper ends thereof are connected to the first and second conductive layers, and the spatial intervals in the arrays of the first and second conductive layers are smaller than those in the arrays of the first and second through-holes.

4. Claims 1 – 3, 6 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Suzuki (PN 5,598,029, of record).

Suzuki discloses, as shown in Figure 4, a semiconductor device comprising,

a first conductive layer (7a) formed of a surface of a semiconductor substrate;

a second conductive layer (7b) which is formed close to the first conductive layer, wherein

the distance between adjacent conductive structures (the first conductive layer (7a) and the second conductive layer (7b)) is commonly determined by the permittivity of the insulating layer (17b,16b) encapsulating the conductive structures. Please note that permittivity of the insulating layer controls the capacitance between adjacent conductive structures. Effective

control of this capacitance is essential in achieving the optimum electrical characteristics of a semiconductor device. So this particular limitation is held inherent in that the distance between the adjacent conductive structures is determined by the permittivity of the insulating layer. In alternative, this limitation (the distance between the adjacent conductive structures being determined by the permittivity of the insulating layer) deals with how the claimed device is made. Therefore, the claimed device must be directed to the product per se, no matter how actually made.

With regard to claim 2, Suzuki discloses the second conductive layer is made of a conductive film being filled in a through hole being located close to the first conductive layer and passing through at least a part of the insulating film; and the first and second conductive layers are connected to first and second potentials, respectively, and a capacitor, which extends in the depth direction of the through hole, is formed by using the insulating inter-layer film interposed between the first conductive layer and the second conductive layer within the through hole.

With regard to claim 3, Suzuki discloses the through hole comprises a second through hole being electrically connected to a semiconductor region or a wiring region only at either of the opened ends thereof.

With regard to claim 6, Suzuki discloses the first conductive layer is formed within a first through-hole being separated by a predetermined distance from the through-hole, whereby a vertical capacitor, which extends in the depth direction of the through-hole, is formed by the first

and second conductive layers (7a,7b) and the insulating film (17b,16b) interposed between the first and second conductive layers.

With regard to claim 17, Suzuki discloses the first and second conductive layers are filled in the first and second through-holes, and the upper ends thereof are connected to the first and second conductive layers, and the spatial intervals in the arrays of the first and second conductive layers are smaller than those in the arrays of the first and second through-holes.

***Response to Arguments***

5. Applicant's arguments filed 07/31/02 have been fully considered but they are not persuasive.

It is argued, at page 8 of the Remarks, that Takahashi patent provides no discussion regarding capacitance permittivity , specific inductive capacitance, dielectric properties of any of the materials of the described device, therefore, it is wholly impossible that the Takahashi device has a distance between a first conductive layer and a second conductive layer that is determined in accordance with a permittivity of an insulating layer. This argument is not convincing because the permittivity of the insulating layer controls the capacitance between adjacent conductive structures. Effective control of this capacitance is essential in achieving the optimum electrical characteristics of a semiconductor device. So this particular limitation is held inherent in that the distance between the adjacent conductive structures is determined by the permittivity of the insulating layer. In alternative, this limitation (the distance between the adjacent conductive structures being determined by the permittivity of the insulating layer) deals with how the

claimed device is made. Therefore, the claimed device must be directed to the product per se, no matter how actually made.

It is argued, at page 8 of the Remarks, that the Nakanishi et al. patent is not a semiconductor device but is instead a carrier for a circuit chip that may be a semiconductor device. In response to applicant's arguments, the recitation a semiconductor device has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951). Further, Nakanishi et al. teaches a chip carrier comprises a semiconductor material and is used to protect the chip from external contaminations, therefore, it is a part of the semiconductor device.

It is argued, at page 8 of the Remarks, that the Suzuki patent is directed to a bypass capacitor that is formed between a gate oxide film 3 and gate 4, and the teachings regarding capacitance have nothing to do with the first and second conductive layers 7a and 7b, and that there is no teaching within the Suzuki patent that is directed to permittivity of any insulating layer. This argument is not convincing because the first and second conductive layers 7a and 7b are used as the power supply line 1 and the ground line 2. Note Col. 6, lines 10-29 of Suzuki. Since the power supply line and the ground line are located near each other, the capacitance will occur between them.

Further, the permittivity of the insulating layer controls the capacitance between adjacent conductive structures. Effective control of this capacitance is essential in achieving the optimum electrical characteristics of a semiconductor device. So this particular limitation is held inherent in that the distance between the adjacent conductive structures is determined by the permittivity of the insulating layer. In alternative, this limitation (the distance between the adjacent conductive structures being determined by the permittivity of the insulating layer) deals with how the claimed device is made. Therefore, the claimed device must be directed to the product per se, no matter how actually made.

*Conclusion*

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung K. Vu whose telephone number is (703) 308-4079. The examiner can normally be reached on Mon-Thurs 7:00-5:30, Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Vu

November 12, 2002

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
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